#12/C 9/24/02 Surla

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Bailey et al.

Docket No.: TI-27935

Serial No.: 09/452,691

Examiner: Fenty, J.

Filed: 12/02/99

Art Unit: 2815

For: AN INTEGRATED CIRCUIT HAVING A THIN FILM RESISTOR LOCATED WITHIN A MULTILEVEL DIELECTRIC BETWEEN AN UPPER AND LOWER METAL INTERCONNECT LAYER

COPY OF PAPERS ORIGINALLY FILED

Amendment under 37 CFR 1.116

Assistant Commissioner of Patents

Washington, DC 20231

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on

Jacqueline J. Garner, Reg. No. 36,144

Dear Sir:

The following amendments and remarks are offered in response to the Examiner's Office Action dated 03/15/02. They are respectfully submitted as a full and complete response to that Action.

Please amend the above-referenced application as follows:

In the Claims:

Please amend claim 1 as follows:

1. (amended) An integrated circuit comprising:

a lower metal interconnect layer located over a semiconductor body;